Remarks

The instant Office Action dated April 28, 2009 notes that prosecution has been re-opened after appeal and listed the following new grounds of rejection: claims 1, 3 and 4 stand rejected under 35 U.S.C. § 103(a) over Dally (U.S. Patent No. 6,192,384) in view of Garde (U.S. Patent No. 6,510,510); and claims 2 and 5-7 stand rejected under 35 U.S.C. § 103(a) over the '384 and '510 references in further view of Fisher (U.S. Patent No. 6,026,479). Applicant traverses all of the rejections and, unless stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully traverses the § 103(a) rejections because the cited '384 reference either alone or in combination with the '510 reference lacks correspondence to the claimed invention. For example, neither of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.,* a first set of issue slots that have holdable registers on the multiple data output paths but not on the single data input path and a second set of issue slots that have holdable registers on the single data input path but not on the multiple data output paths. Because neither reference teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence to the claimed invention. As such, the § 103(a) rejections fail.

More specifically, aspects of the claimed invention are directed to particular placements of holdable registers within a multi-issue processor. As discussed in Applicant's disclosure, multi-issue processors contain multiple functional units. Depending upon the current instruction, one or more of the functional units might not be used each cycle. Thus, one aspect of the invention uses a set of holdable registers located at the input of the functional units (*see, e.g.,* Figure 2). Thus, when a functional unit is not used, the input remains constant, thereby reducing power consumption of the functional unit. Other aspects of the present invention recognize that when an interrupt event occurs, the presence of such holdable registers means that a large amount of data needs to be stored before the interrupt event can be processed. Thus, a second set of holdable registers is implemented before a routing network (*see, e.g.,* Figure 3). The routing network provides multiple data outputs for a single data input and therefore, the total number of registers is less when placed before the routing network. The second set of holdable registers can, for example,

be used in connection with an issue slot that is associated with interrupts (*see, e.g.,* claim 5). Neither of the cited references teaches issue slots that have different configurations of holdable registers, as in the claimed invention. For example, the '384 reference teaches that each of ALU clusters 18 uses the same configuration of buffers 28 (*i.e.,* the asserted holdable registers) with a buffer 28 being located on each output of cross point switch 30 in each of the ALU clusters 18. *See, e.g.,* Figure 1 and 2. The '510 reference also teaches that each of computational blocks 12 and 14 uses the same configuration of latches (*i.e.,* the asserted holdable registers) with a latch 132 being located on the input to buses 110 and 112 and latches 160 and 165 located on the outputs of the buses 110 and 112 in each of the computational blocks 12 and 14. *See, e.g.,* Figures 1 and 2. As such, neither reference teaches issue slots that have different configurations of holdable registers (as claimed) and, thus, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence to the claimed invention.

Moreover, Applicant submits that the '384 reference teaches away from a modification that would remove the buffers (local register files) 28 from some of the ALU clusters 18. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('384) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). The '384 references teaches that the ALU clusters 18 use the local register files 28 to store intermediate results produced during computations within the cluster so they do not need to re-circulate through the stream register 14. *See, e.g.,* Col. 4:7-17. Consistent with the purpose of the '384 reference, the use of the local register files 28 provides a tiered storage architecture thereby reducing bandwidth demands on the stream register file. *See, e.g.*, Col. 2:24-27 and Col. 2:46-51. Thus, removing the local register files 28 from some of the ALU clusters 18 would undermine the operation and the purpose of the '384 reference. Removing the local register files 28 from some of the ALU clusters 18 would also change the principal of operation of the '384 reference. *See, e.g.,* M.P.E.P. § 2143.01 ("If the proposed modification or

invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious."). Accordingly, the '384 reference teaches away from such a modification and the rejections cannot be maintained.

In view of the above, the § 103(a) rejections are improper and Applicant requests that they be withdrawn.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, David Schaeffer, of NXP Corporation at (408) 474-9068 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

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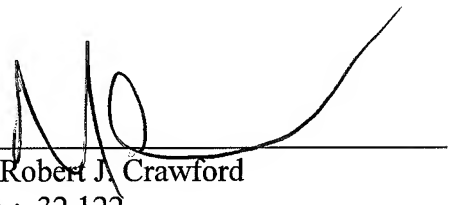
By: 
Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633 x2300
(NXPS.305PA)